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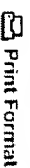
Full chip false timing path identification: applications to the PowerPC™ microprocessors

Jing Zeng   Abadir, M.S.   Bhadra, J.   Abraham, J.A.
ASP Somerset Design Center, Motorola Inc., Austin, TX;

This paper appears in: **Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings**

03/13/2001 -03/16/2001, 2001

Location: Munich, Germany

On page(s): 514-518

2001

References Cited: 11

Number of Pages: xxxvi+829

INSPEC Accession Number: 6964654

Abstract:
Static timing anaylsis sets the industry standard in the design methodology of high speed/performance microprocessors to determine whether timing requirements have been met. Unfortunately, not all the paths identified using such analysis can be sensitized. This leads to a pessimistic estimation of the processor speed. Also, no amount of engineering effort spent on optimizing such paths can improve the timing performance of the chip. In the past we demonstrated initial results of how ATPG techniques can be used to identify false paths efficiently. Due to the gap between the physical design on which the static timing analysis of the chip is bused and the test view on which the ATPG techniques are applied to identify false paths, in many cases only sections of some of the paths in the full-chip were analyzed in our initial results. In this paper, we will fully analyze all the timing paths using the ATPG techniques, thus overcoming the gap between the testing

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Dynamical Identification Of Critical Paths For Iterative Gate Sizing

How-Rem Lin   TingTing Hwang

This paper appears in: **Computer-Aided Design, 1994., IEEE/ACM International Conference on**

On page(s): 481-484
6-10 Nov 1994
ISSN: 1063-6757

Abstract:
Not Available

Index Terms:
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[PDF Full-Text (524 KB)]   DOWNLOAD CITATION

Intervals in software execution cost analysis

Wolf, F. Ernst, R.
Inst. fur Datenverarbeitungsanlagen, Tech. Univ. Braunschweig;

This paper appears in: **System Synthesis, 2000. Proceedings. The 13th
International Symposium on**
09/20/2000 - 09/22/2000, 2000
Location: Madrid, Spain
On page(s): 130-135
2000
References Cited: 14
IEEE Catalog Number: 00TH8500
Number of Pages: xiii+232
INSPEC Accession Number: 6748726

Abstract:
The timing and power consumption of embedded systems are state and input
data-dependent. A formal analysis of such dependencies leads to intervals rather
than single values. These intervals depend on the program properties, execution
paths and states of processes, as well as on the target architecture. This paper
presents an approach to the analysis of process behaviour using intervals. It
improves on previous work by exploiting program segments with single paths and
by taking the execution context into account. The example of an ATM cell handler
demonstrates significant improvements in analysis precision

Index Terms:
asynchronous transfer mode computer architecture embedded systems hardware-software
codesign power consumption software cost estimation telecommunication computing
timing ATM cell handler analysis precision embedded systems execution context
execution paths input data dependence intervals power consumption process behaviour

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Primitive path delay faults: identification and their use in timing analysis

Sivaraman, M.   Strojwas, A.J.
Carnegie Mellon Univ., Pittsburgh, PA;

This paper appears in: **Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on**

On page(s): 1347-1362
Volume: 19,   Issue: 11,   Nov 2000
ISSN: 0278-0070
References Cited: 38
CODEN: ITCSDI
INSPEC Accession Number: 6821021

Abstract:
Present-day digital systems are characterized by large complexity, operation under
tight timing constraints, numerous false paths, and large variations in component
delays. In such a scenario, it is very important to ensure correct temporal behavior
of these circuits, both before and after fabrication. For combinational circuits, it
has been shown that it is necessary and sufficient to guarantee that the primitive
path delay faults (PDFs) are fault-free to ensure that the circuit operates correctly
for some timing constraint T and all larger timing constraints. We show that
primitive PDFs determine the stabilization time of the circuit outputs, based on
which we develop a feasible method to identify the primitive PDFs in a general
multilevel logic circuit. We prove that the maximum primitive PDF delay is exactly
equal to the maximum circuit delay found under the floating mode of operation
assumption. From this result, we devise a method to perform timing analysis
based on primitive PDF identification which delinks functional analysis from delay
computation. Our timing analysis approach provides several advantages over

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A quick and inexpensive method to identify false critical paths using ATPG techniques: an experiment with a PowerPC™ microprocessor

Bhadra, J. Abadir, M.S. Abraham, J.A.

Texas Univ., Austin, TX;

This paper appears in: **Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000**

05/21/2000 - 05/24/2000, 2000

Location: Orlando, FL., USA

On page(s): 71-74

2000

References Cited: 11

IEEE Catalog Number: 00CH37044

Number of Pages: 596

INSPEC Accession Number: 6715330

Abstract:

Static timing analysis tools are used by designers of high speed/high performance circuits to determine whether timing requirements are met. Timing analysis tools can report critical paths which are characterized by a transition on each node along the path, however, they cannot generate a “witness” vector which would sensitize that path. This gives rise to the possibility of having paths which are reported by the static timing analysis tool as potential critical paths, whereas there exists no vector sequence which can sensitize them. Our goal is to identify these “false critical timing paths” safely and without much overhead, so that the efforts needed to redesign and/or optimize critical paths can be reduced. We have devised a simple technique using a tool that we have written

wysiwyg://39/http://search.ieeexplore.ieee.org/searc...Bhadra%2C+J.%3B+Abadir%2C+M.S.%3B+Abraham%2C+J.A.%3B

and a commercial ATPG tool to meet this goal. We applied the technique on the state of the art fourth generation MPC7400 PowerPC™ microprocessor designed at Motorola's PowerPC Design Center in Austin, TX. Our initial experimental results show the effectiveness of the technique. The salient features of the technique are that it is both quick and inexpensive.

Index Terms:
automatic test pattern generation   integrated circuit testing   logic testing   microprocessor chips   timing   ATPG techniques   MPC7400   Motorola   PowerPC microprocessor   false critical paths identification

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Full chip false timing-path identification

Jing Zeng Abadir, M. Bhadra, J. Abraham, J.
Somerset Design Center, Motorola Inc., Austin, TX ;

This paper appears in: **Signal Processing Systems, 2000. SiPS 2000. 2000
IEEE Workshop on**
10/11/2000 -10/13/2000 , 2000
Location: Lafayette, LA, USA
On page(s): 703-711
2000
References Cited: 11
IEEE Catalog Number: 00TH8528
Number of Pages: xv+836
INSPEC Accession Number: 6852719

Abstract:

Static timing analysis sets the industry standard in the design methodology to
gage the speed of high performance microprocessors. Unfortunately, not all the
paths identified using such analysis can be sensitized. This leads to a pessimistic
estimation of processor speed, and the engineering efforts spent optimizing such
paths can not improve the performance of the chip. In the past, we demonstrated
initial results of how ATPG technique can be used to eliminate false paths
efficiently. Due to the gap between the physical design on which the static timing
analysis of the chip is based and the test view on which the ATPG technique is
applied to eliminate false paths, in many cases only sections of some of the paths
in the full-chip were analyzed in our initial results. In this paper, we fully analyze
all the timing paths using the ATPG technique overcoming the gap between the
testing and timing analysis techniques. We applied our method on the second G4
PowerPC™ .

wysiwyg://47/http://search.ieeexplore.ieee.org/searc...Author=Jing+Zeng%3B+Abadir%2C+M.%3B+Abraham%2C+J.%3B

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False timing path identification using ATPG technique and delay-based information

Jing Zeng Abadir, M. Abraham, J.
High Performance Tools & Methodology, Motorola Inc., Austin, TX;

This paper appears in: **Design Automation Conference, 2002. Proceedings.**
39th
On page(s): 562-565
2002
ISSN: 0738-100X

Abstract:
Not Available

Index Terms:
automatic test pattern generation delays formal verification instruction sets integrated
circuit testing logic testing microprocessor chips timing ATPG techniques Motorola
MPC7455 PowerPC instruction set architecture delay information delay-based information
false timing path identification processor speed static timing analysis tools timing
verification total timing paths

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